# PROGRAMMABLE INTER-VIRTUAL CHANNEL AND INTRA-VIRTUAL CHANNEL INSTRUCTIONS ISSUING RULES FOR AN I/O BUS OF A SYSTEM-ON-A-CHIP PROCESSOR

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## ABSTRACT OF THE DISCLOSURE

[050] A method and apparatus for programming instruction issuing rules for instructions residing among various virtual channels, as well as the same virtual channel of an I/O bus interface for a system-on-a-chip processor. In the method and apparatus of the present invention both intra-virtual channel dependencies and inter-virtual channel dependencies are fully programmable, thereby offering significant advantages over prior art I/O interfaces. The method and apparatus of the present invention is broadly comprised of a system for managing data transactions between a first bus and a second bus. A first transaction conversion module is operably connected to the first bus and is operable to receive transactions from the first bus and a first format and to convert those transactions into an internal format. An ordering rules logic module is operably connected to the first transaction conversion module and is further operable to control issuing of transactions in accordance with a dependency relationship between the individual transactions. The ordering rules logic module generates validated transactions that are provided to a second conversion transaction module which is operably connected to the second bus. The ordering rules logic module of the present invention is fully programmable and, therefore, does not need to be redesigned when the data processing system is adapted to operate on a new bus system.